AADL Specification of the ASAAC Communication Architecture

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- Introduction to ASAAC
- The AADL Notation
- ASAAC Modelling Approach #1
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ASAAC >> Common Functional Modules (CFM)

- **DP** ... Data Processing
- **GP** ... Graphics Processing
- **SP** ... Signal Processing
- **MM** ... Mass Memory
- **NS** ... Network Switch
- **PC** ... Power Conversion
MSU ... Module Support Unit
RU ... Routing Unit
NIU ... Network Interface Unit
DP ... Data Processing (Payload)
ASAAC >> Graphics Processing Module (GPM)

MSB ... Module Support Board
CB ... Communications Board
PB1 ... Payload Board #1
PB2 ... Payload Board #2

ETN  FC  ATM  Display

MSB  CB  PB1  PB2
ASAAC >> SW Architecture (Comms Part)

Application Layer (AL)
- App #1
- App #2
- App #3

OS Layer (OSL)
- Virtual Channel Manager (VCM)
- Config Manager (CM)
- Blueprint Manager (BPM)

Module Support (MSL)
- Network Independent Interface (NII) Communications Implementation

APOS ... Application to Operating System Interface
MOS ... Module to Operating System Interface
SMOS ... System Management to Operating System Interface
SMBP ... System Management to Blueprint Interface
ASAAC >> SW Integration

Application Layer (AL)

OS Layer (OSL)

Module Support (MSL)

MSB

CB

PB

Message Router

Buffer Handler

NiiMsi Handler

Application

APOS

VCM & GSM

MOS

PB

ATM

FC

DP

EADS Military Aircraft
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AADL Graphical Primitives >> Components

Software
- Data
- Thread
- Process

Platform
- Device
- Memory
- Processor

Composite
- System

Bus
AADL Graphical Primitives >> Features

- Data Port
- Event Port
- Event Data Port

Ports

- Immediate
- Delayed

Connections

Client / Server

client -> server
Approach #1 >> Common Functional Module (CFM)

CFM.DpmVme

MSB [PowerPCBoard]
  Memory
  PowerPC
  PCI

CB [PowerPCComms]
  ATMBoard
  Memory
  PowerPC
  PCI

PB [PowerPCBoard]
  Memory
  PowerPC
  PCI

Backplane [VME]

ETH

ATM

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Approach #1 >> Module Support Layer (MSL)

MSL.DpmVme

- Message Router
- Buffer Handler
- NilMsl Handler

CFM.DpmVme

- MSB
- CB
- PB

- ETH
- ATM

MOS

- MOS_configureInterface
- MOS_configureTransfer
- MOS_configureNetwork
- MOS_sendTransfer
- MOS_receiveTransfer
- MOS_destroyTransfer
- MOS_networkStatus
- MOS_networkInfo
Approach #1 >> Operating System Layer (OSL)

OSL.DpmVme

- VCM
- CM
- BPM
- MOS
- SMBP
- SMOS

APOS
- APOS_sendMessageNonblocking
- APOS_receiveMessageNonblocking
- APOS_sendMessage
- APOS_receiveMessage
- APOS_lockBuffer
- APOS_sendBuffer
- APOS_receiveBuffer
- APOS_unlockBuffer
- APOS_waitOnMultiChannel

CFM
- MSB
- CR
- PB

ETH
- ATM
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Approach #1 >> Application (Reader/Writer)

ASAACApplication.RW

Reader

CPP.DpmVme

APOS_sendMessage

APOS_receiveMessage

Writer

DPM1

DPM2

ATM0
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Approach #2 >> Common Functional Module (CFM)

CFM.DpmVme

MSB [PowerPCBoard]
- Memory
- PowerPC

CB [PowerPCComms]
- Memory
- PowerPC
- ATMBoard

PB [PowerPCBoard]
- Memory
- PowerPC

Backplane [VME]

ETH

ATM
Approach #2 >> Module Support Layer (MSL)

MSL.DpmVme

Message Router

Buffer Handler

NiiMsl Handler

MOS
- MOS_configureInterface
- MOS_configureTransfer
- MOS_configureNetwork
- MOS_sendTransfer
- MOS_receiveTransfer
- MOS_destroyTransfer
- MOS_networkStatus
- MOS_networkInfo
Approach #2 >> Operating System Layer (OSL)

- OSL.DpmVme
- VCM
- SMOS
- SMBP
- MOS
- APOS
  - APOS_sendMessageNonblocking
  - APOS_receiveMessageNonblocking
  - APOS_sendMessage
  - APOS_receiveMessage
  - APOS_lockBuffer
  - APOS_sendBuffer
  - APOS_receiveBuffer
  - APOS_unlockBuffer
  - APOS_waitOnMultiChannel
Approach #2 >> Application (Reader/Writer)

ASAACApplication.RW

Reader

Writer

APOS_sendMessage

APOS_receiveMessage

CPP.DpmVme

DPM1

DPM2

ATM0
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Approach #3 >> System Component Refinement

Step 1
Refinement of system component P2

Step 2
Refinement of system component P1
Approach #3 >> Application (Reader/Writer)

ASAACApplication.RW

Virtual Channel (Connection)

Reader

Writer

CPP_APOS.Abstract

APOS_sendMessage

APOS_receiveMessage

DPM_APOS (Abstract Processor)

DPM_APOS (Abstract Processor)

Transfer Connections (Logical Bus)
Approach #3 >> CPP_APOS Refined

CPP_APOS_Refined

Transfer Connection (Connection)

MOS_sendTransfer

MOS_receiveTransfer

ATM Channels (Logical Bus)
Approach #3 >> CPP_MOS Refined

CPP_MOS.Refined

ATM Channel (Connection)

CPP_HW.Abstract

DPM_HW

MSB  CB  PB

Backplane[VME]

DPM_HW

MSB  CB  PB

Backplane[VME]

ATM0 (Physical Bus)
Approach #3 >> Vertical Refinement Problem

DPM_APOS (Abstract Processor) refined

DPM_APOS

DPM_MOS (Abstract Processor)

SMOS

SMBP

BPM

MOS

VCM
Approach #3 >> Vertical Refinement Problem (cont’d)

Further refinement impossible!
(system boundary problem)
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Open Issues

- No explicit modelling of communication on application and operating system level in approaches #1 & #2 (without step-wise refinement)

- No clear relation between subprogram calls and ports, i.e. relation between control flow and data flow

- Modelling of OSI-conform multi layered communication is possible in terms of step-wise refinement. However, vertical and horizontal refinement can not be applied at the same time.