



# Presentation of Spices



*Support for Predictable Integration  
of mission Critical Embedded Systems*

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# Part I

## Overview of the project



# Consortium and figures

- European ITEA project with France, Spain and Belgium
- Partners:
  - Airbus, Axlog, CEA, Féria, Lester, THALES Avionics, THALES communications, Verimag
  - Barco, Cetic, K.U. Leuven
  - SQS, U. Cantabria
- From 2006-09-01 to 2009-08-31
- Budget: 16 M€

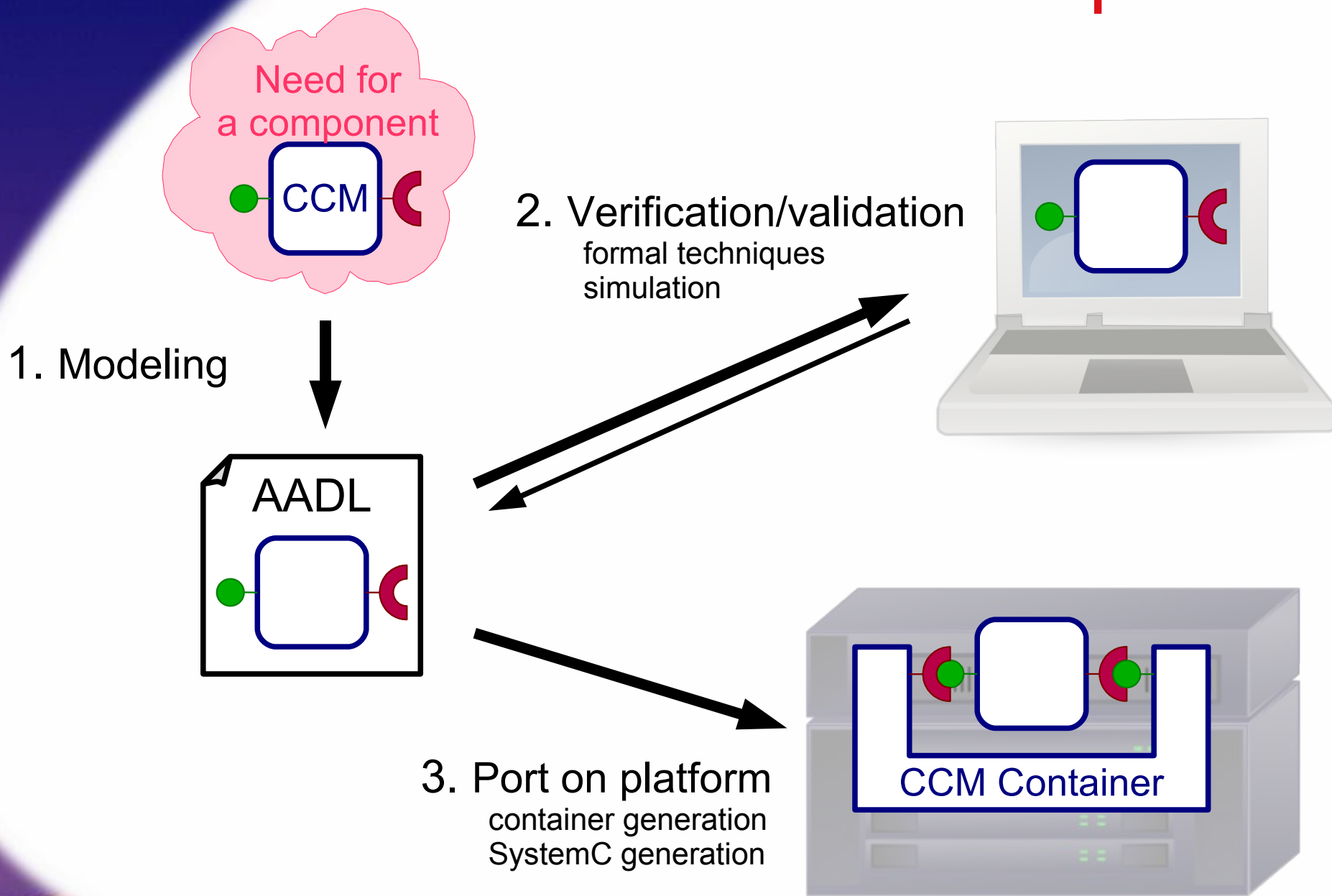


# Goals

- *The principal goals of SPICES are to extend the capacities of the microCCM component-based framework and to couple it with an AADL modeller in order to offer to system architects, software architects and applications designers a component-based modelling, design and analysis environment for distributed real-time embedded systems that should be deployed over heterogeneous targets such as GPP, DSP or FPGA*



# Aimed process

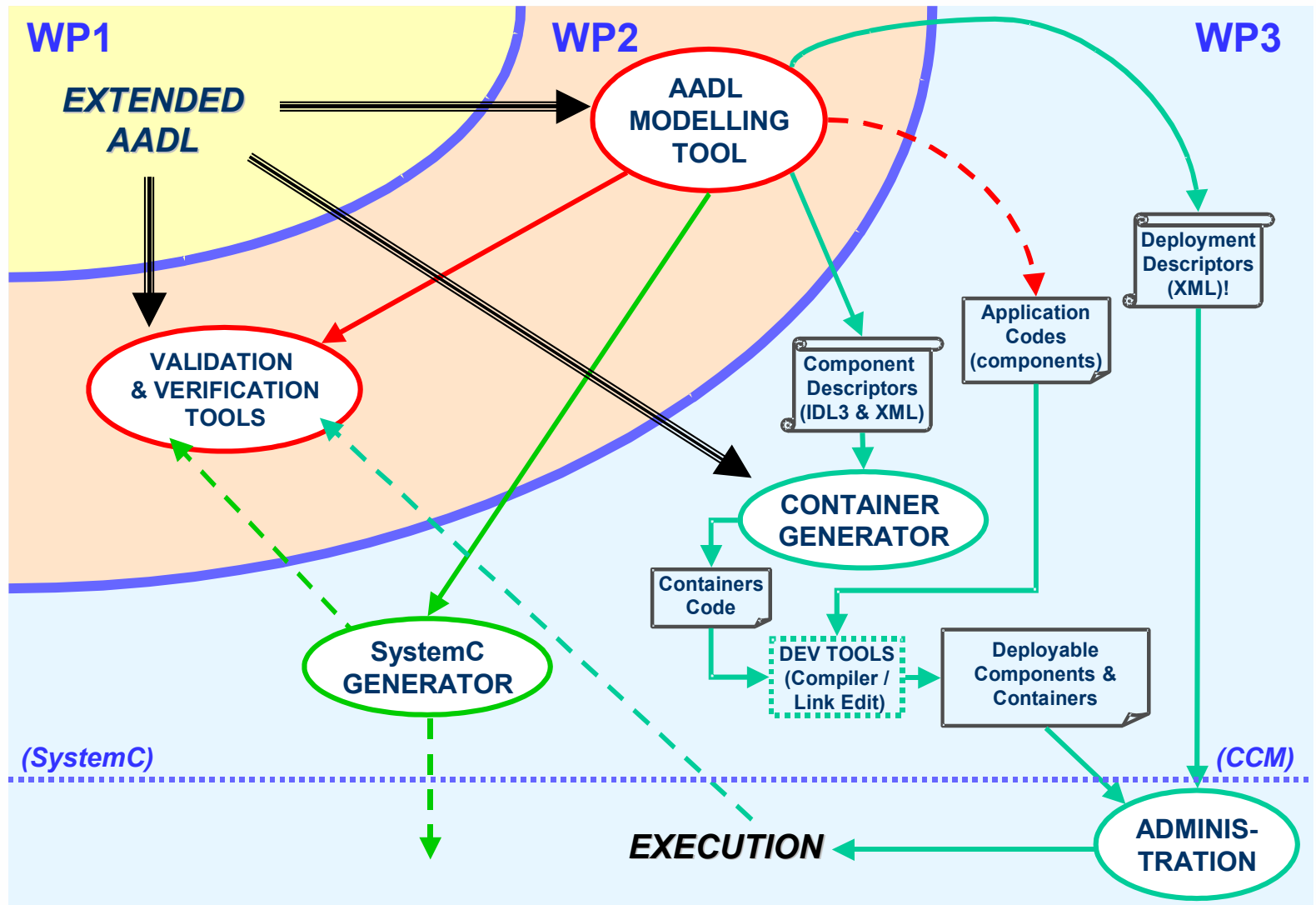




# Organization of the project

- WP1: How to model CCM components with AADL  
*(step 1 of the process)*
- WP2: Which verifications and validations, development of the tools to support them  
*(step 2 of the process)*
- WP3: How to port on the target platform, development of the tools to support it  
*(step 3 of the process)*
- WP4: Case studies
- WP5: Dissemination

# Organization of the project





- Modeling CCM with AADL
  - Method guide, new property sets, new annexes
- Verification/validation tools integrated with OSATE
  - Simulation
  - Qualification of CCM components
  - WCET measure and prediction
  - Power consumption prediction
- Porting on target platform
  - Generation of CCM descriptors
  - AADL to SystemC translator



# Contributions to AADL

- Static properties
  - Modeling CCM
  - Power consumption
- Dynamic properties
  - Behavior annex
- Core language improvement
  - Feedback from case studies
- Tool developments
- Dissemination and promotion



## Preliminary requirements for AADL



# Some general requirements expressed by partners

- Describe the behavior of the system external environment
- Describe the main temporal constraints and/or performances of the system
- Hierarchically design the system as a component-based application
- Describe hierarchically the hardware architecture and its associated runtime environment
- Specify the deployment plan of the application on the hardware architecture and its runtime environment, including dynamic reconfiguration constraints



# Impact on AADL

- Need for a **methodology** to use AADL
- Modeling of CCM components and interfaces (facets/receptacles and event exchanges)
  - Impact on subprogram concept
- Modeling of hardware aspects
  - Problem with current semantics rules of devices
  - Support for DSPs, FPGAs, ASICs, etc.
- Many new specific AADL properties
  - Temporal constraints, power consumption, etc.