ADeS presentation

a simulator for AADL
v0.2.2

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Agenda

- Objective of the simulation
- Presentation of the tool
- Demonstration
- To go further
Objective of the simulation
Why simulating AADL?

- Scheduling analysis
- Mode change analysis
- Workload statistics
- Temporal dimensioning
- Data flow study
- Control flow study

ADeS
Behavior simulation of AADL architecture
Requirements for a simulator

- Simulation of the full AADL specification with exact compliance with the standard
- Support of behavior descriptions
- Support of AADL extensibility (new properties, new protocols, etc.)
- Integration with other AADL tools
- Storage of the results for post-analyses
Area of the simulation

- Components
  - Individual behavior
- Communication between components
  - Bus & data access
  - Subprogram calls
  - Port connections
- Modes
  - Local mode change
  - SOM change
Presentation of the tool
Technical overview

- ADeS
  - Eclipse plug-in
  - Built on OSATE and Topcased
  - Interoperability with AADL tools
  - Under Eclipse Public License
Behavior description

AADL standard behavior

Simulation kernel

Scheduling protocols
Queuing protocols
...
Objective: provide a minimal behavior description
Target: threads, devices, subprograms
Form: list of sequential actions
Possible actions:
- Compute (<duration>)
- Raise (<port>)
- Raise (<port>, <data>)

```plaintext
annex behavior {**
  t1 {  
    compute(10);  
    raise(chMode);
  } in modes (normal);
  t1 {  
    compute(25);  
    raise(chMode);
  } in modes (backup);
**};
```
Flexibility and extensions

- Support of AADL annexes
  - Capability to develop new supports
- Capability to add of new protocols
  - scheduling protocols
  - dispatch protocols
  - dequeuing protocols
  - overflow handling protocols
  - queue processing protocols
- Possibility to reuse of the core level for other simulation models
Demonstration
Driving a simulation

OSATE

AADL modeling

Check of the AADL model

ADeS

ADeS needs fulfilled?

Yes

Instantiation

Simulation

No
Demo scenario 1

Proc A
- Sched. protocol = RMS
  - TA1: 100ms, CET=35ms
  - TA2: 150ms, CET=45ms
  - TA3: 200ms, CET=25ms

Proc B
- Sched. protocol = RMS
  - TB1: 40ms, CET=10ms
  - TB2: 60ms, CET=15ms
  - TB3: 80ms, CET=20ms

Mem

SI
Demo scenario 2

- **t1**: 20ms/60ms CET=10ms/25ms
- **t2**: 100ms CET=20ms

**proc**
- Sched. protocol = RMS

**mem**

**dev**
- prop. delay = 5ms

**b**
- backup

**S.I**
- normal
To go further
Design of a new GUI

**Navigator**

- System
- Process
  - Thread sender
    - Dispatch
    - Complete
    - Error
    - triggerPort
  - Thread receiver
    - Dispatch
    - Complete
    - Error
    - triggerPort
- Processor
- Memory

**Editor**

- Display depending on the selected component
- Current status
- Display options
- Breakpoints

**Properties**

<table>
<thead>
<tr>
<th>Property</th>
<th>Value</th>
</tr>
</thead>
</table>

**Chronograms**

- Console

- sender
- receiver
- processor
Road map

2006

• Strengthening of simulation kernel
• Improvement of AADL compliance
• Trace mechanism

2007

• Demo version for trial
• New GUI
• Support of behavior annex
• New developments on demand

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More information

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